REMARKS

In addition to the remarks filed on November 28, 2003, Applicants respectfully submit the following as further evidence that ***Ando*** would not render the current invention obvious under 35 U.S.C. §103 if combined with admitted prior art of the application.

According to ***Ando***, as shown in Fig. 7A and 7B, the non-doped channel layer 63, InGaAs, is provided between the buffer layer 2, i-GaAs, and the electron supply layer 64, n-AlGaAs. And the channel layer 63 is a multiple of quantum well layers which have a third energy band gap having a variation in a perpendicular direction to the interfaces with a minimum value (maximum of fraction x of In) at a portion except for adjacent portions to the interfaces. This definition is written on lines 37-51 of column 8 of Ando. The layers correspond to this definition in that the first potential barrier is the electron supply layer 64, n-AlGaAs, the second potential barrier is the buffer layer 2, i-GaAs, and the quantum well layers are the non-doped channel layer 63, InGaAs.

Further, according to the definition written from line 61 of column 8 to line 2 of column 9 of ***Ando***, the third compound semiconductor material (the non-doped channel layer 63) comprises $In_xGa_{1-x}As$, the fraction x of In having a variation in a perpendicular direction to the interfaces with the maximum value at a portion not adjacent to portions of the interfaces, for example, a portion having a distance in the range from 30 angstroms to 110 angstroms from the interface to the first potential barrier. Further, a step-graded variation of the fraction x of In in the ternary compound InxGa1-xAs is available.

Therefore, according to the invention of ***Ando***, the InGaAs layer 63B with the maximum value of fraction x of In should be away from the interface to the electron supply layer 64, n-AlGaAs, with a range from 30 to 110 angstroms, as shown in Fig. 7B. The third compound semiconductor material should have step-graded quantum well layers 63E, 63D and 63C between the layer 63B and the electron supply layer 64, n-AlGaAs, with the same step-graded quantum well layer 63A between the layer 63B and the buffer layer 2, i-GaAs. The reason for this requirement is that the InGaAs layer is not lattice-matched with the substrate 1, GaAs, the buffer layer 2, i-GaAs, nor the electron supply layer 64, n-GaAs. Therefore, according to ***Ando***, the channel layer 63 should not have a larger thickness than the critical thickness with which the channel layer 63, InGaAs, can be lattice-matched with the adjacent layers, even though the material is not lattice-matched with the adjacent layers. In Ando, the step-graded quantum well layers of 63A-63E can have a larger thickness and the fraction x of In can be larger than the non-step-graded layer 3, InGaAs, shown in Fig. 1B and 1C of Ando.

Therefore, ***Ando*** clearly teaches away from combining its invention with the admitted prior art of Fig. 6 in which the channel layer 104, InGaAs, is in contact with the electron supply layer 106, InAlAs, via the thin spacer layer 105.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 50-2866.

Respectfully submitted,

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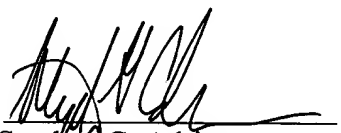
By: 

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